

Accurate Prediction of PHEMT Intermodulation Distortion Using the Nonlinear Discrete Convolution Model

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Abstract — A general-purpose, technology-independent behavioral model is adopted for the intermodulation performance prediction of PHEMT devices. The model can be easily identified since its nonlinear functions are directly related to conventional DC and small-signal differential parameter measurements. Experimental results which confirm the model accuracy at high operating frequencies are provided in the paper.

I. INTRODUCTION

Different approaches [1..7] have been proposed in the literature for the look-up-table based nonlinear dynamic modeling of electron devices. Their basic aim is that of providing accurate large-signal performance prediction directly in terms of conventional experimental data (i.e., I/V characteristics and bias dependent small-signal AC measurements), without the need for equivalent circuits and technology-dependent analytical functions to describe the device characteristics.

The empirical model adopted in this paper, beside preserving the same kind of approach, efficiently exploits the interpolation algorithm proposed in [8] for the accurate prediction of intermodulation distortion (IMD) in PHEMT devices. This is a key aspect for the design of the highly-linear power amplifiers required in many modern communication systems, taking also into account that many models available in the literature and/or provided by the foundries often fail in IMD prediction.

The proposed model is based on a purely behavioral functional description which can be strongly simplified by considering that the relation between currents and voltages in an electron device only involves memory effects which are short with respect to its typical operating frequencies. This hypothesis is well verified for devices not affected by strong parasitics or after parasitic de-embedding as confirmed by two-dimensional numerical simulations and actual measurements. In such conditions, a finite-memory model, with a suitably chosen memory time T_M , can be adopted without introducing important

approximations in the dynamic device response [2]. It could be demonstrated that quasi-static models are a special case of finite memory models with $T_M \rightarrow 0$.

The proposed model, which is particularly suitable for the implementation in commercial microwave CAD tools, can be directly identified on the bases of conventional measurements and least-square parameter extraction algorithms.

II. THE NONLINEAR DISCRETE CONVOLUTION MODEL

The time-domain current/voltage relationship of a single port electron device can be expressed as:

$$i(t) = \lim_{T_M \rightarrow \infty} \Psi|v(t-\tau), V_0|_{\tau=0}^{T_M} \quad (1)$$

where Ψ is a suitable nonlinear functional or "line-function", which formally represents the nonlinear dependence of the electron device current i at the generic instant t on the present and past values of the applied voltage $v(t-\tau)$ over a virtually infinite memory time-interval T_M . The dependence of the current $i(t)$ on the DC component V_0 of the voltage has been introduced to describe in a simplified way, according to the approaches proposed in [9,10,11], the low-frequency dispersive phenomena due to "traps". This is important in order to separate the "long lasting" memory of the charge "trapping" phenomena from the relatively "short" memory dynamics associated with all the other charge storage phenomena within the device. In fact, the main simplification which leads to our model derives from the basic hypothesis that, apart from low-frequency dispersion and linear parasitics which can be modeled separately, all the other device dynamics is limited to a memory time T_M which is not only practically finite, but also relatively short (i.e., much shorter than the period of the typical operating signals). The validity of such an hypothesis has been verified for a large family of almost intrinsic devices (i.e., devices not affected by strong parasitics, or after de-

embedding from parasitics), both through accurate numerical device simulations and experimental results.

When the short memory condition is satisfied, so that a small T_M can be used in (1) without introducing any relevant "memory truncation error", the device dynamics can be more conveniently described in terms of "dynamic voltage deviations" $e(t, \tau) = v(t-\tau) - v(t)$, suitably defined as the difference between the "past" value $v(t-\tau)$ of the applied voltage with respect to the present value $v(t)$:

$$i(t) \approx \Phi \left| v(t), e(t, \tau), V_0 \right|_{\tau=0}^{T_M} \quad (2)$$

If the time value T_M is short enough in relation to the operating frequency of the applied voltage, the deviations $e(t, \tau)$ can be considered small even under large signal conditions, so that the nonlinear functional dependence on $e(t, \tau)$ in (2) can be described in terms of a linear convolution with respect to $e(t, \tau)$:

$$i(t) = F^{LF} [v(t), V_0] + \int_0^{T_M} g[v(t), \tau] [v(t-\tau) - v(t)] d\tau \quad (3)$$

The term $F^{LF}[v(t), V_0]$ in (3) describes the device behavior at DC and low-frequency operation by taking also into account the effects of dispersive phenomena through the additional dependence on the mean value V_0 of the applied voltage [9,10,11]. The second term in (3) represents a purely-dynamic single-fold convolution integral between voltage deviations and a "pulse response function" $g[v(t), \tau]$ nonlinearly-controlled by the instantaneous applied voltage. This term accounts for purely-dynamic nonlinear phenomena which are important at high operating frequencies.

Equation (3) represents a finite memory nonlinear model which correctly describes the behavior of a given electron device provided that suitable values of T_M can be found for which the errors due to both memory truncation and linearization with respect to the voltage dynamic deviations are small enough [2].

In order to make model extraction and implementation feasible, the memory time $[0, T_M]$ of the nonlinear intrinsic device is divided into a suitable number N_D of intervals of width $\Delta\tau$. This allows for a new formulation of the model where the dynamic deviation is a function of a finite number of points in the τ -domain, while the voltage-controlled dynamic pulse response is expressed by means of a p index which "discretizes" the convolution integral by a finite summation:

$$i^e(t) = F^{LF} [v(t), V_0] + \sum_{p=1}^{N_D} g_p [v(t)] [v(t - p\Delta\tau) - v(t)] + \Delta i_{par}(t) \quad (4)$$

In this expression an additional current contribution $\Delta i_{par}(t)$ has also been included in order to account for the possible presence of a parallel parasitic linear network, as shown in Fig.1 for the two-port case. The parasitic term in (4) can be explicated in the following form:

$$\Delta i_{par}(t) = \sum_{p=N_D+1}^{N_{DL}} \Delta y_p [v(t - p\Delta\tau) - v(t)] \quad (5)$$

In fact, it is reasonable to assume that not only the active intrinsic device but also the parasitic linear network can be described in the time domain in terms of the intrinsic voltage through a convolution integral over the finite time T_{ML} . The terms Δy_p are the $(N_{DL} - N_D)$ pulse response samples of the parasitic network corresponding to each elementary time interval of its memory T_{ML} . Since the parallel parasitic network is linear, there is no need for any "short" memory constraint. Thus, for better model accuracy, values of T_{ML} which are still finite but quite longer than T_M can be chosen. Moreover, without loss of generality, the parasitic network pulse response has been assumed equal to zero over the short memory interval $[0, T_M]$; this in order to avoid ambiguities in model extraction, owing to the parallel connection of the parasitic network with the intrinsic transistor.

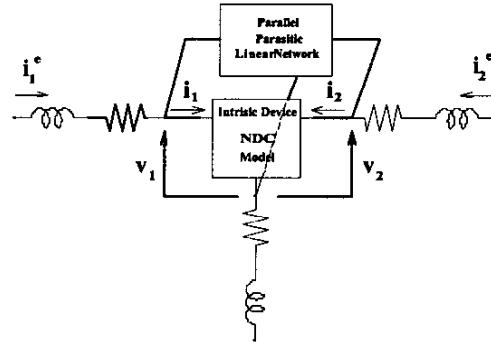


Fig.1. Equivalent scheme for parasitic modeling in the Nonlinear Discrete Convolution model.

Equation (4) represents the general purpose Nonlinear Discrete Convolution (NDC) model capable of accurately predict the dynamic behavior for different electron devices under large-signal operating conditions. It can be easily identified starting from conventional I/V characteristics and bias dependent small-signal parameter measurements, while its analytical form allows for a simple and systematic implementation in microwave circuit simulators such as Agilent-ADS.

III. MODEL IDENTIFICATION

The model extraction procedure simply starts from DC and pulsed I/V characteristic measurements [9] on the device, which lead to the identification¹ of the F^{LF} term in (4). Then, the “weights” $g_p[v(t)]$ and Δy_p of the voltage dynamic deviations can be computed for any value of the controlling voltage $v(t)=V_B=V_0$ by minimizing the mean square discrepancy between the measured small-signal admittance $Y_{mis}[V_B, \omega]$ ($i=1, \dots, N_\omega$) and the corresponding value predicted by model (4). More precisely, by linearizing and Fourier transforming (4), the model “fitting” to the measured intrinsic admittance $Y_{mis}[V_B, \omega]$ can be expressed in the form:

$$Y_{mis}[V_B, \omega_i] = g^{LF}[V_B] + \sum_{p=1}^{N_D} g_p[V_B] \left[e^{-j\omega_i p \Delta\tau} - 1 \right] + \sum_{p=N_D+1}^{N_B} \Delta y_p \left[e^{-j\omega_i p \Delta\tau} - 1 \right] \quad (6)$$

where $g^{LF}[V_B]$ is the differential conductance corresponding to the low-frequency term F^{LF} .

When a suitably wide set of different bias points V_B ($k=1, \dots, N_B$) and frequencies ω_i ($i=1, \dots, N_\omega$) has been chosen, expression (6) provides a set of $N_B \times N_\omega$ complex equations, which impose the congruence between the model small-signal response and the measured admittance Y_{mis} . It should be noted that these equations are linear with respect to the $N_{DL} + (N_B - 1)N_D$ unknowns $g_p[V_B]$, for $k=1, \dots, N_B$, $p=1, \dots, N_D$ and with respect to Δy_p for $p=N_D + 1, \dots, N_{DL}$ which are the characteristic parameters of the purely dynamic part of the NDC model. Thus, the model extraction procedure can be based on simple and reliable algorithms for the mean-square solution of over determined systems of linear equations. This is an important advantage with respect to conventional models, whose parameter extraction normally involves nonlinear optimization algorithms, which may suffer from different convergence problems, like the strong dependence on the starting point due to multiple local minima. Our model, instead, involves a much larger number of parameters, but their extraction from measured data can be carried out with simple and highly reliable numerical techniques.

The model extraction procedure enables the voltage-controlled terms $g_p[v]$ to be computed only over a grid of voltages $v=V_B$ within the device operating region, thus providing only a sampled characterization of the nonlinear model functions. Clearly, since continuous and highly

¹As an alternative the approaches proposed in [10,11], which do not require pulsed I/V measurements, can be applied.

regular functions are needed for accurate circuit simulation, suitable general-purpose methods for the interpolation or approximation of nonlinear functions defined by look-up tables are needed. In particular, a previously proposed approach for nonlinear function approximation, based on sampled-signal theory [8], was adopted for its high flexibility in accurately describing different nonlinear electron device characteristics.

All the above expressions, which have been presented by considering for simplicity a single-port electron device, can be easily generalized to multiport devices by vector re-interpretation.

IV. EXPERIMENTAL RESULTS

In this paper experimental results concerning the NDC model capabilities for IMD prediction are provided. In particular, the model has been applied for the nonlinear modelling of a $0.25 \times 600 \mu m$ PHEMT device to be used in the design of highly linear amplifiers for both point to point and point to multipoint microwave links.

First, the DC characteristics and small-signal S-parameter measurements have been de-embedded from parasitic resistances and inductances. Then the NDC model and the parallel linear parasitic network were identified, on the basis of the procedure outlined above, by using $T_M=6ps$, $N_D=3$ ($\Delta\tau=2ps$), $N_{DL}=30$.

Figure 2 shows the IMD to carrier ratio, as a function of the output power, measured and predicted through the NDC model at 13 and 15GHz (the two tone displacement was 10MHz and the device was biased in class A with $I_D=60mA$, $V_{DS}=6.5V$). Despite the very low level of the IMD products (required by the specific application), the NDC prediction shows an excellent agreement with experimental data for a wide number of load and source impedance conditions.

V. CONCLUSION

The Nonlinear Discrete Convolution model has been applied for the intermodulation prediction of PHEMT devices. One of the main feature of the model is its systematic and unambiguous identification procedure. More precisely, the “fitting equations” which impose the constraints between the model response and actual measurements are linearly dependent on model parameters, so that a conventional least-square algorithm can be adopted for their identification.

As confirmed by the experimental results presented, the model provides accurate results in IMD prediction at high operating frequencies. Future work will be devoted to model validation in the Ka band.

REFERENCES

- [1] F.Filicori, G.Vannini, V.A.Monaco, "A nonlinear integral model of electron devices for HB circuit analysis", IEEE Trans. on MTT, Jul 1992.
- [2] F.Filicori, A.Santarelli, P.Traverso, G.Vannini, "Electron device model based on nonlinear discrete convolution for large-signal circuit analysis using commercial CAD packages", Proc. of GAAS99, Munich, Germany, Oct 1999.
- [3] D.E.Root et al., "Technology independent large-signal non quasi-static FET models by direct construction from automatically characterized device data", Proc. of 21st EuMC, Sep 1991.
- [4] R.Daniels, A.Yang, J.Harrang, "A universal large/small signal 3-terminal FET model using a non quasi-static charge-based approach", IEEE Trans. on ED, Oct 1993.
- [5] Wei CJ et al., "Table-based dynamic FET model assembled from small-signal models", IEEE Trans. on MTT, Jun 1999.
- [6] Angelov I. et al., "An empirical table-based FET model", IEEE Trans. on MTT, Dec 1999.
- [7] M. Fernandez-Barciela et al., "A simplified broad-band large-signal non quasi-static table-based FET model", IEEE Trans. on MTT, Mar 2000.
- [8] F.Filicori, G.Vannini, A.Santarelli, P.Traverso, "A signal-theory based approach for the approximation of electron device characteristics", Proc. of GAAS98, Oct 1998.
- [9] F.Filicori et al., "Empirical modeling of low-frequency dispersive effects due to traps and thermal phenomena in III-V FETs", IEEE Trans. on MTT, Dec 1995.
- [10] A.Santarelli, F.Filicori, G.Vannini, P.Rinaldi, "Backgating model including self-heating for low-frequency dispersive effects in III-V FETs", Electronics Letters, Oct 1998.
- [11] A.Santarelli et al., "Equivalent-voltage description of low-frequency dispersive effects in large-signal FET models", Proc. of GAAS2001, Gallium Arsenide Applications Symposium, London, UK, Sept 2001.

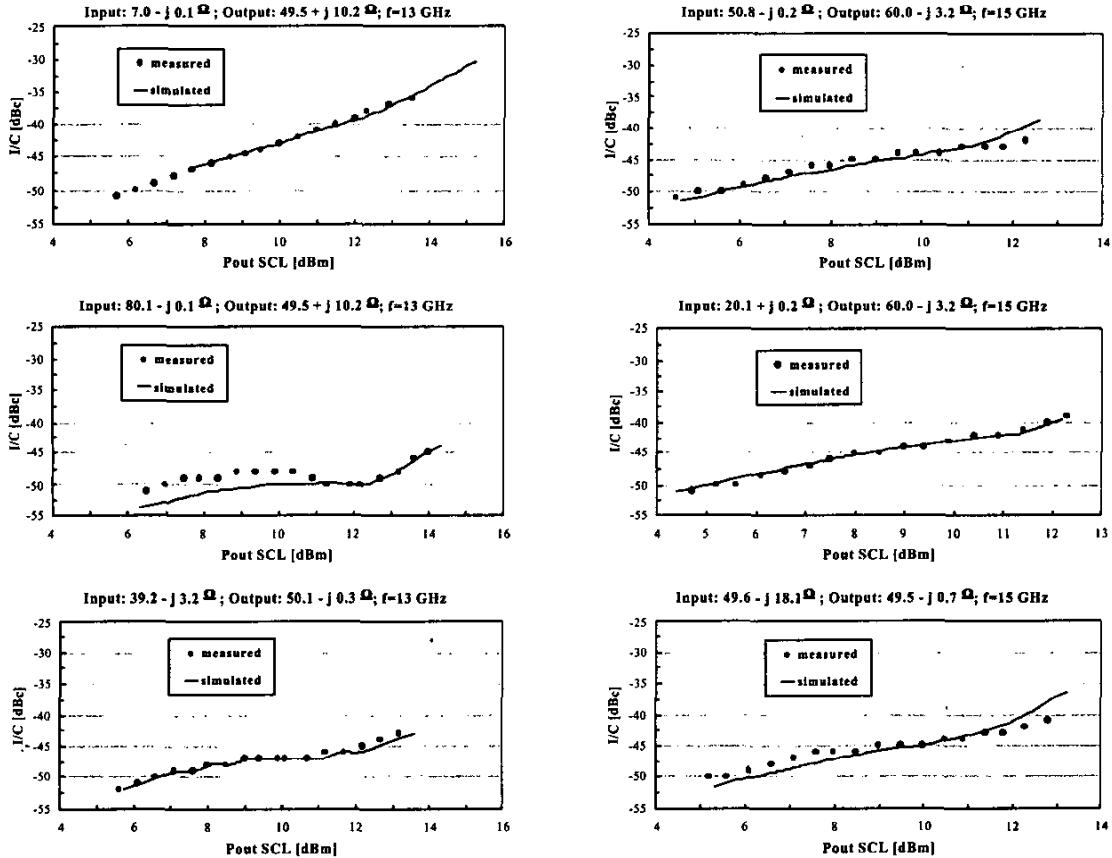


Fig.2 - IMD to carrier ratio vs. output power (Single Carrier Level), measured (•) and predicted through the NDC model (—) at 13 and 15GHz, corresponding to different input and output terminations.